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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	PAPER NUMBER
2185	19

DATE MAILED: 08/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRE

Office Action Summary	Application No.	Applicant(s)	
	09/477,034	DOVER ET AL.	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003 amendments* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 48-76 are presented for examination.

Specification

2. Claim 70 is objected to because of the following informalities: in last paragraph, the phrase "second value_used" should have been "second_value used." Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 48-76 are rejected under 35 U.S.C. 102(b) as being anticipated by Incardona et al (EP 274045 A1[1]).

4. As per claim 48, Incardona et al teach

maintaining a first value for a first counter based on a content of a volatile memory [abstract; fig. 1, volatile memory 13; col. 1, lines 49-50; col. 2, lines 16-22];

[1] Reference cited in the prior office action, paper no 16.

maintaining a second value for a second counter based on a content of a non-volatile memory [abstract; fig. 1, non-volatile memory 20; col. 1, lines 44-47; col. 2, lines 33-38]; and

controlling updates to the first value for the first counter and to the second value for the second counter, the first and second values used to generate a monotonic counter [abstract; col. 1, lines 17-34; an electronic odometer].

5. As per claims 49, 60, 71 and 75, Incardona et al teach updating the second value for the second counter when the first value for the first counter meets a predetermined condition [col. 4, lines 25-32; col. 7, lines 1-7].

6. As per claim 50, Incardona et al teach reading the first value for the first counter and the second value for the second counter, wherein the controlling comprises updating the first value for the first counter in response to the reading of the monotonic count [fig. 1; display unit 27; col. 2, lines 45-51; inherently display unit reads out the value for displaying before control unit updates the value of the first counter].

7. As per claims 51, 61, 72 and 76, Incardona et al teach that the controlling comprises updating the second value upon a power on reset [inherent to the system as to maintain the current up to date value; col. 3, lines 3-10; col. 4, lines 25-32].

8. As per claims 52, 62, 65 and 68, Incardona et al teach updating the second value by programming a bit location or location in a flash memory [col. 4, lines 36-42; bit burning].

9. As per claim 53, Incardona et al teach updating the second value by updating a portion of a flash memory when another portion of the flash memory meets a predetermined condition [col. 4, lines 36-42; recording of a 100 km increment].

10. As per claims 54 and 56, Incardona et al teach

the monotonic counter at least partially basing the count value on a content of a volatile memory and a non-volatile memory [abstract; col. 6, lines 17-34]; and

utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value [abstract; col. 5, lines 41-48; col. 6, lines 17-34].

11. As per claims 55 and 57, Incardona et al teach updating the count value for the monotonic counter comprises updating a flash memory to update the non-volatile memory [inherent to the system as a flash memory is a type of non-volatile memory; abstract; col. 6, lines 17-34].

12. As per claim 58, Incardona et al teach

a volatile counter to maintain a first value [abstract; fig. 1; volatile memory 13; col. 6, lines 17-34];

a non-volatile counter to maintain a second value based on a content of a non-volatile memory [abstract; fig. 1; non-volatile memory 20; col. 6, lines 17-34]; and

control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic count [abstract; col. 5, lines 41-48; col. 6, lines 17-34].

13. As per claims 59 and 74, Incardona et al teach that the control logic controls the volatile counter to update the first value when the first and second values are read [fig. 1; display unit 27; col. 2, lines 45-51; inherently display unit reads out the values for displaying before control unit updates the first value].

14. As per claim 63, Incardona et al teach that the non-volatile memory is separated into more than one block [inherently as non-volatile memory is programmed in sequence; col. 4, lines 36-42].

15. As per claims 64 and 67, Incardona et al teach

a volatile memory to maintain a first value for a first counter [abstract; fig. 1; volatile memory 13; col. 6, lines 17-34];

a non-volatile memory to maintain a second value for a second counter [abstract; fig. 1; non-volatile memory 20; col. 6, lines 17-34]; and

circuit to maintain a count value for a monotonic counter [abstract; col. 5, lines 41-48; col. 6, lines 17-34].

16. As per claims 66 and 69, Incardona et al teach the non-volatile memory comprises a first block of flash memory and a second block of flash memory and wherein the circuitry updates the second block of flash memory and erases the first block of flash memory when a predetermined condition is met [col. 4, lines 36-58; inherently flash memory is a type of non-volatile memory].

17. As per claim 70, Incardona et al teach

one or more registers to store a first value [abstract; fig. 1; volatile memory 13; col. 6, lines 17-34];

a first adder to maintain the first value [inherent in the system as incrementing the count];

a flash memory to store a portion of bits used for a monotonic count [abstract; fig. 1; non-volatile memory 20; col. 6, lines 17-34];

one or more registers to store a second value [fig. 1; decoder 21 and decoder 22; col. 4, line 46 – col. 5, line 13];

a second adder to [inherent in the system as incrementing the count]; and

a control engine to control the flash memory and the first and second adders, the firs_value used to determine lower significant bits of the monotonic count and the second_value used to determine higher significant bits of the monotonic count, the lesser significant bits being volatile while higher significant bits being non-volatile [abstract; abstract; col. 5, lines 41-48; col. 6, lines 17-34].

18. As per claim 73, Incardona et al teach

a monotonic counter comprising:

a volatile counter to maintain a first value [abstract; fig. 1; volatile memory 13; col. 6, lines 17-34];

a non-volatile counter to maintain a second value [abstract; fig. 1; non-volatile memory 20; col. 6, lines 17-34], and

control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic count [abstract; col. 5, lines 41-48; col. 6, lines 17-34]; and

one or more processors to read the first and second values [col. 2, lines 7-26; processor unit].

Response to Arguments

19. Applicant's arguments with respect to claims 48-76 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

sks

August 11, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100